UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,838	04/15/2004	Peidong Wang	AHURA-10	6853

7590 07/11/2006

Mark J. Pandiscio
Pandiscio & Pandiscio, P.C.
470 Totten Pond Road
Waltham, MA 02451-1914

EXAMINER	
REAMES, MATTHEW L	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,838	WANG ET AL.	
	Examiner	Art Unit	
	Matthew L. Reames	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-82 and 84* is/are pending in the application.

4a) Of the above claim(s) *47-54,68 and 82* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-46,55-67,84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 4/16/04 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species A in the reply filed on 6/8/2006 is acknowledged.

Claim Objections

2. Claims 41,46,64,65 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

a. As to claim 41,46, the structure of 40 would inherently have three\four different photoluminescence shift since as the band gap shift so does the photoluminescence.

b. As to claim 64 and 65, any anneal process has to take place at a certain temperature and for a certain time.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 36,42,55,61,66,67,84 are rejected under 35 U.S.C. 102(b) as being anticipated by Poole (US 6,027,989).

a. As to claim 36 and 84, Poole teaches a method for forming a semiconductor substrate, the method comprising: providing a single semiconductor wafer having a first end and a second end in opposition to one another, a longitudinal axis formed between the first end and the second end, a top surface and a bottom surface in opposition to one another (see fig. 9a), a plurality of quantum wells disposed in the semiconductor wafer, and the plurality of quantum wells having a given bandgap (see fig. 9a); depositing a first dielectric cap on a first given portion of the top surface of the single semiconductor wafer (see item 12); and rapid thermal annealing of the first dielectric cap deposited on the top surface of the single semiconductor material to tune the plurality of quantum wells disposed beneath the first dielectric cap from the given bandgap to a first tuned bandgap (see fig. 9a) ; wherein the first tuned bandgap is greater than the given bandgap (see fig. 9a and column 5 lines 20-30).

b. As to claim 42 Poole teaches wherein the mask only covers a portion of the semiconductor substrate leaving a uncapped portion (see fig. 9a)

c. As to claim 55 and 61, Poole teaches a mask made from SiO2 (see claim 3).

d. As to claims 66 and 67, Poole teaches 700 degrees C (see claim 6).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 37,38,43,44,45,56,57,58,60,62,63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poole.

a. As to claim 37, Poole teaches a temporary mask item 12, which at least partially covers the semiconductor.

Poole does not explicitly teach wherein the top surface of the single semiconductor is entirely covered by the first given portion.

However it would have been obvious to one of ordinary skill in art at the time of the invention to form layer 12 over the entire surface then to pattern the mask.

One would have been so motivated since this is a standard method for forming and patterning masks.

b. As to claim 38,43, Poole teaches a step further comprising the steps of depositing a second dielectric cap on the top surface of the single semiconductor wafer subsequent to the step of rapid thermal annealing of the first dielectric cap (see column 5 lines 30-40), the second dielectric cap configured to cover a second given portion of the top surface wafer (see fig. 9a item 14), and rapid thermal annealing of the second dielectric cap deposited on the top surface of the single semiconductor material to further tune the plurality of quantum wells disposed beneath the second dielectric cap from the first tuned bandgap to a second tuned bandgap (see fig. 9a and column 5 lines 20-30), wherein the second tuned bandgap is greater than the first tuned bandgap (see fig. 9a).

Poole does not teach wherein the second mask is smaller then the first.

However it would have been obvious to one of ordinary skill in the art at the time of the invention to make the second mask smaller then the first.

One would have been so motivated for the desire of different sized region (i.e. heavy region medium region and light region).

c. As to claims 56,57,62,63, Poole does not explicitly teach how the mask is formed however it would have been obvious to one of ordinary skill in the art at the time of the invention to use either ion or electron beam sputtering.

One would have been so motivated since these are standard deposition methods and would have therefore provided a cost benefit.

d. As to claims 58, Poole teaches wherein the first section comprises a first given photoluminescence shift corresponding to the given bandgap, the second section comprises a second given photoluminescence shift corresponding to the first tuned bandgap, the third section comprises a photoluminescence shift corresponding to the second tuned bandgap, and a fourth section comprises a fourth given photoluminescence corresponding to a third tuned bandgap (see fig. 9a).

e. As to claim 60 Poole teaches, wherein the single semiconductor wafer further comprises multiple laser sources formed by the first section, the second section, the third section, and the fourth section, respectively (column 3 lines 30-50).

6. Claims 39,40,59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poole.

a. As to claim 39,44, Poole does not teach a step further comprising the steps of depositing a third dielectric cap on the top surface of the single semiconductor wafer subsequent to the step of rapid thermal annealing of the second dielectric cap, the third dielectric cap configured to cover a third given portion of the top surface of the single semiconductor wafer, the third given portion configured within the second given portion, the third given portion having a smaller surface area than the second given portion, and rapid thermal annealing of the third dielectric cap deposited on the top surface of the single

semiconductor material to further tune the plurality of quantum walls disposed beneath the third dielectric cap from the second tuned bandgap to a third tuned bandgap, wherein the third tuned bandgap is greater than the second tuned bandgap.

However it would have been obvious to one of ordinary skill in the art at the time of the invention to repeat the steps of Poole a third time.

One would have been so motivated to a greater variation in the wavelengths of light, say a fifth at a higher energy then the other four.

b. As to claim 40,45, modified Poole teaches wherein the single semiconductor wafer comprises a first section, a second section, and a third section and a fourth section, the first section consisting of the plurality of quantum wells disposed beneath the first portion exclusive of the second portion, the second section consisting of the plurality of quantum wells disposed beneath the second portion exclusive of the third portion, and the third section consisting of the plurality of quantum wells disposed beneath the third portion, wherein the first section has the first tuned bandgap, the second section has the second tuned bandgap, and the third section has the third tuned bandgap (see eg fig. 9a).

c. As to claim 59, Poole does not explicitly teach exciting each individual section to tune the regions.

However it would have been obvious to one of ordinary skill in the art at the time of the invention to pump each region individually.

One would have been so motivated to test the output frequencies.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew L. Reames whose telephone number is (571)272-2408. The examiner can normally be reached on M-Th 6:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MLR

BRADLEY BAUMEISTER
PRIMARY EXAMINER